REMARKS

Claims 1-21 are pending in this application. Claims 9-13 have been allowed, and claims 2, 4-7 and 15-20 have been objected to for containing allowable subject matter. Claims 1, 3, 8 and 14 have been rejected under art. Claims 1, 9, 14 and 21 are independent. Reconsideration of the rejection is respectfully requested.

Allowable Subject Matter

Applicants appreciate that claims 9-13 and 21 are allowed, and claims 2-7 and 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the features of the base claim and any intervening claims. However, it is respectfully submitted that claims 1, 8 and 14-15 are also allowable in view of the following remarks.

Claim Rejection – 35 U.S.C. § 102

Claims 1, 8, 14 and 15 are rejected under 35 U.S.C. § 102(b) as being anticipated by Takaya, U.S. Patent No. 5,783,967. The rejection is respectfully traversed.

Independent claim 1 recites, *inter alia*, a control circuit that detects a phase difference between the first clock signal and the delayed clock signal, and outputs a control signal to the delay circuit corresponding to the detected phase difference.

As shown in an example, non-limiting embodiment of the invention, Fig. 2 illustrates a control circuit 230 having a phase detector 231, a comparator 232 and a counter 233. The phase detector 231 receives a first clock signal CLK 1 and a delayed clock signal CLKD, detects a phase difference between the signals, and then outputs a first voltage V1 and a second voltage V2 to the comparator 232 reflecting the detected phase difference. The

comparator 232 compares the first voltage V1 and the second voltage V2, and outputs to the counter 233 a logic signal having a predetermined logic state based on the result of the comparison. When the difference between the first voltage V1 and the second voltage V2 is greater than a predetermined value, the comparator 232 outputs a signal for increasing the output signal of the counter 233. When the difference between the first voltage V1 and the second voltage V2 is less than the predetermined value, the comparator 232 then outputs a signal for decreasing the output signal of the counter 233. Thus, the counter 233 receives the signal output from the comparator 232 and outputs the control signal CTRL to the delay circuit 210. The control signal CTRL is received as an input to the delay circuit 210 for controlling the time delay applied by the delay circuit 210.

Takaya fails to disclose or suggest a control circuit that detects a phase difference and outputs a control signal to the delay circuit corresponding to the detected phase difference, as recited in claim 1.

Takaya discloses in Fig. 2 a multiplier circuit having a first and second voltage control delay circuits 22, 23, a phase comparator 24 for comparing the phase of the input signal with the phase of an output signal of the second voltage control delay circuit 23, a loop filter 25 responsive to the output signal of the phase comparator 24 for producing a control signal for controlling the first and second voltage control delay circuits 22, 23 to automatically correct a delay thereof such that an input signal passing through the first and second voltage control delay circuits 23, 24 is delayed in phase by 180°, and an exclusive OR circuit 26 receptive of the input signal and the output signal of the first voltage control delay circuit 22 for outputting a doubled frequency output signal having a duty ratio of 50% (col. 2, lines 26-35 and col. 3, lines 43-49). However, Applicants' submit that the control circuit of Takaya does not detect a phase difference, and outputs a control signal corresponding to the detected phase difference, as recited in Applicants' claim 1. That is, the control signal in

Takaya merely corrects the delay of voltage control delay circuits so as to be in phase with the input signal (column 2, lines 27-31), whereas Applicants' invention discloses outputting a control signal that corresponds to the detected phase difference.

Further, Takaya fails to disclose or suggest the control signal controls a duration of the time delay applied to the first clock signal by the delay circuit, as recited in claim 1.

Takaya is completely silent with regard to controlling the duration of the time delay of the control signal. Takaya merely discloses automatically correcting the delay of two voltage control delay circuits 22, 23 so that the output signal passes through the voltage control delay circuits 22, 23 are delayed 180 degrees in phase from the input signal.

Accordingly, Takaya fails to teach or suggested a control circuit that controls a phase difference between the first class signal and the delayed clock signal, and outputs a control signal to the delay circuit corresponding to the detected phase difference, wherein the control signal controls a duration of the time delay applied to the first clock signal by the delay circuit, as recited in claim 1.

Accordingly, for at least this reason, claim 1 and those claims dependent thereon are allowable over the applied art. Withdrawal of the rejection is respectfully requested.

Regarding claim 14, Applicants submit for similar reasons to those stated above with regard to claim 1, that claim 14 and those claims dependent thereon are also allowable over the applied art. Withdrawal of the rejection is also respectfully requested.

Accordingly, Applicants respectfully submit that for at least the reasons stated above, all currently pending claims 1-21 are now in condition for allowance. Withdrawal of any outstanding rejections and allowance of these claims are respectfully requested.

CONCLUSION

Accordingly, in view of the above remarks, reconsideration of the objections and rejections and allowance of each of claims 1-21 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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